

CLAIMS

1. A method for producing a chip-scale
5 electronic package carried out at the substrate level,
with the substrate (22, 42, 72) being made up of at
least one chip with this said chip having input/output
pads (23, 43, 73) on a substrate face known as the
front face, with the method including the following
10 steps:

a) formation, using a complex mould or stencil, of an
insulating stress relaxation layer (28, 48, 78) on the
aforementioned front face, with the aforementioned
relaxation layer covering the front face of the
15 substrate with a relief surface which provides access
wells to input/output pads and as well as protruding
parts designed to relax stresses, with each protruding
part having a tiered shape made up of at least one
protuberant zone and at least one zone which is
20 recessed relative to the aforementioned protuberant
zone and is intended to support an electrical bonding
pad (30, 40),
b) formation of electrically conductive tracks (25, 45,
75) on the relaxation layer to connect input/output
25 pads to the corresponding electrical bonding pads,
c) formation of means of electrical contact (27, 47,
77) with the exterior on the electrical bonding pads.

2. A method according to claim 1 further
30 including, between steps b) and c), a step for the
formation of an encapsulation layer (29, 49, 79) on the

relaxation layer with the exposure of the electrical bonding pads.

3. A method according to claim 1 in which,
5 to form the stress relaxation layer (28, 48, 78) using a mould, the following steps are followed:

- 1) fill the mould with a given relaxation polymer or apply the said polymer directly onto the front face of the substrate,
- 10 2) align the mould on the front face of the substrate,
- 3) press the mould on the front face of the substrate,
- 4) cure the polymer,
- 15 5) remove the mould.

4. A method according to claim 1 in which, to form the stress relaxation layer (28, 48, 78) using a stencil, the following steps are followed:

- 20 1) apply the stencil to the front face of the substrate,
- 2) fill the orifices in the stencil with a given relaxation polymer,
- 3) cure the polymer and separate the stencil from the

25 substrate.

5. A method according to claim 3 or 4 in which the aforementioned given relaxation polymer is selected from amongst polyimide, BCB or any other
30 polymer capable of relieving stresses.

6. A method according to claim 3 or 4 in which, after the stress relaxation layer (28, 48, 78) is obtained on the front face of the substrate, polymer residues found on the input/output pads (23, 43, 73) 5 are removed.

7. A method according to claim 1, in which the formation step for electrically conductive tracks (25, 45, 75) includes the following steps:
10 a) deposit of a conductive material on the front face of the substrate covered with the relaxation layer (28, 48, 78),
b) separation of the rerouting lines and formation of the electrical bonding pads (30, 40) by removal of
15 conductive material located at the protuberant zone(s) of the protruding parts of the relaxation layer by mechanical lapping or by mechanical-chemical polishing.

8. A method according to claim 1 in which
20 the formation step for electrically conductive tracks (25, 45, 75) is performed by chemical deposition of conductive material in access wells for input/output pads and in zones that are recessed in relation to the protuberant zone(s) of the protruding parts of the
25 relaxation layer (28, 48, 78).

9. A method according to the preceding claim in which the conductive material is a metal.

10. A method according to claim 1 in which the formation step for electrically conductive tracks (25, 45, 75) includes the following steps:

- 5 a) deposit of a conductive material on the front face of the substrate covered with the relaxation layer,
- b) lithography,
- c) chemical etching,
- d) stripping.

10 11. A method according to any of claims 7 and 10, in which the deposition of conductive material involves metallization.

15 12. A method according to claim 1 in which the formation step for electrically conductive tracks (25, 45, 75) includes the following steps:

- a) lithographic metallization of the front face of the substrate covered with the relaxation layer,
- b) electrolysis,
- 20 c) stripping,
- d) chemical etching.

13. A method according to claim 2, in which the formation step for the encapsulation layer (29, 49, 25 79) includes the following steps:

- a) deposit of a layer of polymer over the entire front face of the substrate covered with the relaxation layer,
- b) levelling of the front face of the substrate,
- c) exposure of the electrical bonding pads (30, 40)

14. A method according to claim 2 in which the formation step for the encapsulation layer (29, 49, 79) includes the following steps:

- 5 a) levelling of the front face of the substrate,
- 5 b) filling the access wells and recessed zones in the front face of the substrate with a thick polymer layer,
- c) exposure of the electrical bonding pads (30, 40).

10 15. A method according to claim 1 in which the means of electrical contact (27, 47, 77) with the exterior on the electrical bonding pads (30, 40) are fusible balls.

15 20. A method according to the previous claim in which the fusible balls are introduced onto the electrical bonding pads (30, 40) using a technique selected from electrolysis of a fusible alloy, screen-printing of solder paste and ball transfer.

20 25. A method according to claim 1 in which the means of electrical contact (27, 47, 77) with the exterior on the electrical bonding pads (30, 40) are selected from amongst anisotropic conductive films and adhesives.

25 30. A method according to any of claims 1 and 2, further including a step for separation of electronic chip-scale packages created at the substrate level.

19. A method according to claim 1 in which, before or after the formation of the means of electrical contact (27, 47, 77) with the exterior on the electrical bonding pads, the rear face of the 5 substrate (22, 42, 72) is made thinner by lapping, mechanical-chemical polishing or any other technique.

20. A method according to any of claims 1 and 2, which is supplemented by the following steps:
10 a) the creation of slots in the rear face of the substrate (42) until the metallic layers represented by the integrated circuit input-output pads (43) or by electrically conductive tracks (45) are reached,
b) deposition, possibly localised, of a metallic layer 15 (55) on the rear face of the substrate,
c) removal of the metallization located on the surface of the rear face of the substrate.

21. A complex mould or stencil 20 characterised in that it is designed to create a chip-scale package using the method described in any of claims 1 to 20.

22. A complex mould or stencil according to 25 claim 21, which is made using at least one technique from amongst wet or dry etching, electroforming, adhesion of several pierced or un-pierced polymer films, moulding, laser etching.

23. A complex mould or stencil according to claim 21 or 22, which is made from silicon, metal, polymer.

5 24. A chip-scale package manufactured at the substrate level characterised in that it is created using the method according to any of claims 1 to 20.